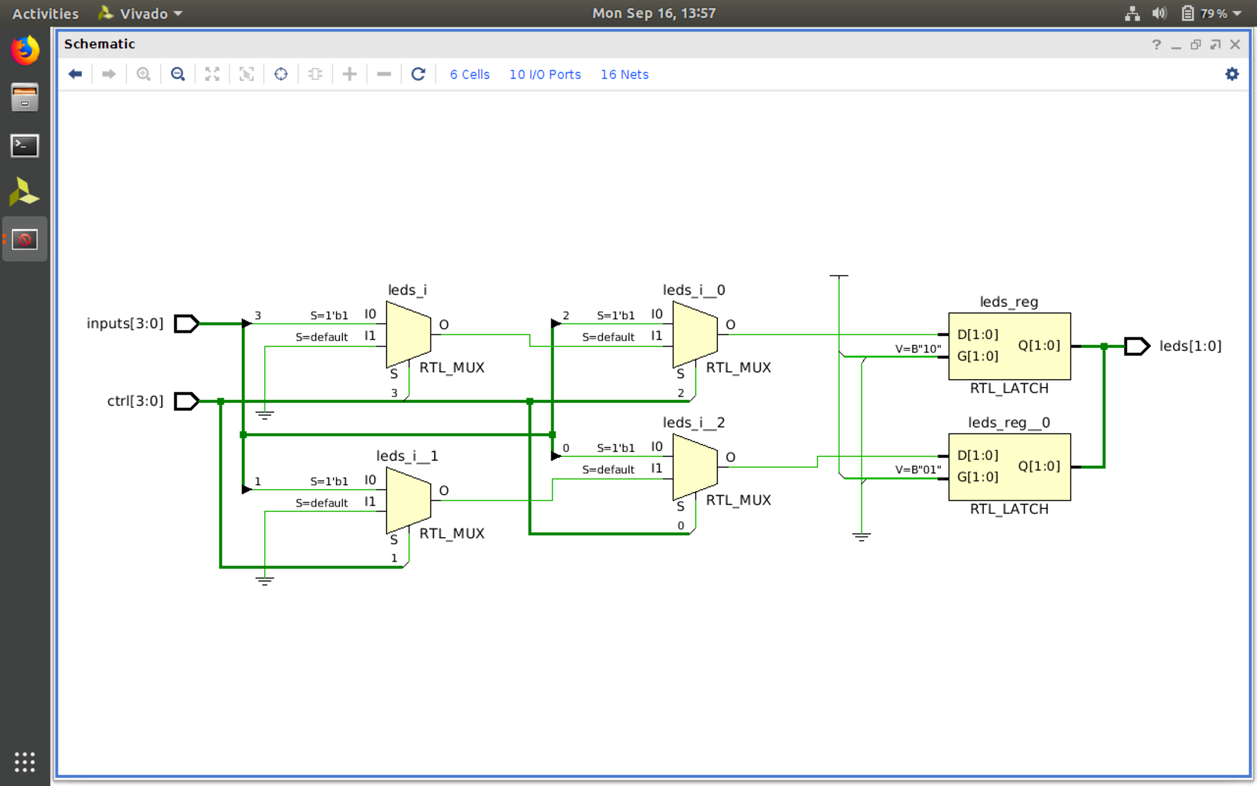
ECE338

Lab #3: Behavioral-to-Schematic Translation, Priority MUX constructs

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For Lab #3, we were tasked with implementing a priority MUX assignment within a process block that first assigns a conditional value to our signal outside the process block, then assigns subsequent values to inside the process block. We made sure to follow the Golden Rules (i.e. all signals read in process blocks are in the sensitivity list, last assignments take precedent, all assignments have default values, no signals are on both sides of equations, and we only assigned a value outside the process block once).



In the Synthesized Design Schematic, all of the multiplexers are represented by LUTs (lookup tables). This provides us with a detailed view of our behavioral VHDL code, as we see *ctrl* and *inputs* each receive the different possible combinations which are then parsed through to LUTs.

